That which is claimed is:

1. A metal-semiconductor field-effect transistor comprising:

a semi-insulating silicon carbide substrate which is substantially free of deep level dopants;

an n-type epitaxial layer of n-type conductivity silicon carbide on the substrate,

ohmic contacts on the n-type epitaxial layer that respectively define a source and a drain; and

a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain to form an active channel in the n-type epitaxial layer between the source and the drain when a bias is applied to the Schottky metal contact.

2. A metal-semiconductor field-effect transistor according to Claim 1, wherein the semi-insulating substrate has a level of deep level dopants which is below a level which dominates the resistivity of the substrate.

3. A metal-semiconductor field-effect transistor according to Claim 1, wherein the semi-insulating silicon carbide substrate has less than about 1×10^{16} cm^{-3} of heavy metals, transition elements and deep level trapping elements.

4. A metal-semiconductor field-effect transistor according to Claim 1, wherein the semi-insulating silicon carbide substrate has less than about 1×10^{14} cm^{-3} of heavy metals, transition elements and deep level trapping elements.

5. A metal-semiconductor field-effect transistor according to Claim 1, further comprising:

a cap layer of n-type silicon carbide on the n-type epitaxial layer;

a first recess in the cap layer;

a second recess in the n-type epitaxial layer, wherein the recess in the n-type epitaxial layer is within the first recess in the cap layer

a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain to form an active channel in the n-type epitaxial layer between the source and the drain when a bias is

applied to the Schottky metal contact wherein the Schottky metal contact is within the recess in the n-type epitaxial layer.

6. A metal-semiconductor field-effect transistor according to Claim 5, wherein the n-type epitaxial layer and the cap layer have carrier concentrations which are substantially the same.

7. A transistor according to Claim 5, wherein the recess in the n-type epitaxial layer extends to a depth of from about 20 nm to about 120 nm.

8. A transistor according to Claim 5, wherein the cap layer has a dopant level from about 1×10^{15} cm^{-3} to about 5×10^{17} cm^{-3}.

9. A transistor according to Claim 5, wherein the cap layer has a thickness of from about 50 nm to about 300 nm.

10. A transistor according to Claim 1, wherein the ohmic contacts are directly on the n-type epitaxial layer.

11. A transistor according to Claim 1, further comprising regions of n^+ silicon carbide between the n-type epitaxial layer and the ohmic contacts.

12. A transistor according to Claim 1, wherein the ohmic contacts comprise nickel contacts directly on the n-type epitaxial layer.

13. A transistor according to Claim 1 further comprising an overlayer on the ohmic contacts and the Schottky metal contact.

14. A transistor according to Claim 13, wherein the ohmic contacts comprise nickel and wherein the overlayer comprises layers of titanium, platinum and gold.

15. A transistor according to Claim 1, wherein the n-type epitaxial forms a mesa having sidewalls extending through the n-type layer which define the periphery of the transistor.

16. A transistor according to Claim 15 wherein the mesa further comprises the substrate and the sidewalls of the mesa extend into the substrate.

17. A transistor according to Claim 15, further comprising a passivation layer on the sidewalls of the mesa and exposed portions of the n-type epitaxial layer.

18. A transistor according to Claim 17, wherein the passivation layer is an ONO passivation layer.

19. A transistor according to Claim 1, further comprising metallization formed on the substrate opposite the n-type layer.

20. A transistor according to Claim 19, wherein the substrate has a thickness of about 100 μm or less.

21. A transistor according to Claim 19, wherein the metallization comprises layers of titanium, platinum and gold coated with an overlayer of eutectic alloy of AuGe.

22. A transistor according to Claim 1 wherein the Schottky metal contact comprises a first gate layer of chromium directly on the n-type epitaxial layer.

23. A transistor according to Claim 22, wherein the Schottky metal contact further comprises an overlayer on the first gate layer, wherein the overlayer comprises layers of platinum and gold.

24. A transistor according to Claim 23, wherein the Schottky metal contact is a mushroom gate.

25. A transistor according to Claim 24, further comprising a recess in the n-type epitaxial layer and wherein the first gate layer is formed in the recess in the n-type epitaxial layer.

26. A transistor according to Claim 24, wherein the mushroom gate is self aligned with respect to the recess.

27. A transistor according to Claim 1, further comprising an undoped silicon carbide buffer layer formed between the substrate and the n-type epitaxial layer.

28. A transistor according to Claim 1, further comprising an n-type conductivity silicon carbide buffer layer formed between the substrate and the n-type epitaxial layer.

29. A transistor according to Claim 1, further comprising a p-type silicon carbide buffer layer formed between the substrate and the n-type epitaxial layer.

30. A transistor according to Claim 29, further comprising an ohmic contact formed on the p-type epitaxial layer.

31. A transistor according to Claim 30, further comprising a well region of p^+ silicon carbide formed in the p-type epitaxial layer and wherein the ohmic contact is formed on the p^+ well region.

32. A transistor according to Claim 30, wherein the p-type epitaxial layer comprises:

a first p-type epitaxial layer; and

a second p-type epitaxial layer, wherein the first p-type epitaxial layer has a doping concentration higher than a doping concentration of the second p-type epitaxial layer.

33. A metal-semiconductor field-effect transistor comprising:

a silicon carbide substrate;

an n-type epitaxial layer of n-type conductivity silicon carbide on the substrate;

ohmic contacts on the n-type epitaxial layer that respectively define a source and a drain;

a cap layer of n-type silicon carbide on the n-type epitaxial layer;

a first recess in the cap layer;

a second recess in the n-type epitaxial layer, wherein the recess in the n-type epitaxial layer is within the first recess in the cap layer; and

a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain to form an active channel in the n-type epitaxial layer between the source and the drain when a bias is applied to the Schottky metal contact wherein the Schottky metal contact is within the recess in the n-type epitaxial layer.

34. A metal-semiconductor field-effect transistor according to Claim 33, wherein the n-type epitaxial layer and the cap layer have carrier concentrations which are substantially the same

35. A transistor according to Claim 33, wherein the recess in the n-type epitaxial layer extends to a depth of from about 20 nm to about 120 nm.

36. A transistor according to Claim 33, wherein the cap layer has a dopant level from about 1×10^{15} cm^{-3} to about 5×10^{17} cm^{-3}.

37. A transistor according to Claim 33, wherein the cap layer has a thickness of from about 50 nm to about 300 nm.

38. A transistor according to Claim 33, wherein the ohmic contacts are directly on the n-type epitaxial layer.

39. A transistor according to Claim 33, further comprising regions of n^+ silicon carbide between the n-type epitaxial layer and the ohmic contacts.

40. A transistor according to Claim 33, wherein the ohmic contacts comprise nickel contacts directly on the n-type epitaxial layer.

41. A transistor according to Claim 33 further comprising an overlayer on the ohmic contacts and the Schottky metal contact.

42. A transistor according to Claim 41, wherein the ohmic contacts comprise nickel and wherein the overlayer comprises layers of titanium, platinum and gold.

43. A transistor according to Claim 33, wherein the n-type epitaxial forms a mesa having sidewalls extending through the n-type layer which define the periphery of the transistor.

44. A transistor according to Claim 43 wherein the mesa further comprises the substrate and the sidewalls of the mesa extend into the substrate.

45. A transistor according to Claim 43, further comprising a passivation layer on the sidewalls of the mesa and exposed portions of the n-type epitaxial layer.

46. A transistor according to Claim 45, wherein the passivation layer is an ONO passivation layer.

47. A transistor according to Claim 33, further comprising metallization formed on the substrate opposite the n-type layer.

48. A transistor according to Claim 47, wherein the substrate has a thickness of about 100 μm or less.

49. A transistor according to Claim 47, wherein the metallization comprises layers of titanium, platinum and gold coated with an overlayer of eutectic alloy of AuGe.

50. A transistor according to Claim 33 wherein the Schottky metal contact comprises a first gate layer of chromium directly on the n-type epitaxial layer.

51. A transistor according to Claim 50, wherein the Schottky metal contact further comprises an overlayer on the first gate layer, wherein the overlayer comprises layers of platinum and gold.

52. A transistor according to Claim 51, wherein the Schottky metal contact is a mushroom gate.

53. A transistor according to Claim 52, wherein the mushroom gate is self aligned with respect to the second recess.

54. A transistor according to Claim 33, further comprising an undoped silicon carbide buffer layer formed between the substrate and the n-type epitaxial layer.

55. A transistor according to Claim 33, further comprising an n-type conductivity silicon carbide buffer layer formed between the substrate and the n-type epitaxial layer.

56. A transistor according to Claim 33, further comprising a p-type silicon carbide buffer layer formed between the substrate and the n-type epitaxial layer.

57. A transistor according to Claim 56, further comprising an ohmic contact formed on the p-type epitaxial layer.

58. A transistor according to Claim 57, further comprising a well region of p^+ silicon carbide formed in the p-type epitaxial layer and wherein the ohmic contact is formed on the p^+ well region.

59. A transistor according to Claim 57, wherein the p-type epitaxial layer comprises:

a first p-type epitaxial layer; and

a second p-type epitaxial layer, wherein the first p-type epitaxial layer has a doping concentration higher than a doping concentration of the second p-type epitaxial layer.

60. A metal-semiconductor field-effect transistor comprising:

a bulk single crystal silicon carbide substrate;

an n-type epitaxial layer of n-type conductivity silicon carbide on the substrate;

a p-type epitaxial layer of selectively doped p-type conductivity silicon carbide between the substrate and the n-type epitaxial layer, wherein the p-type conductivity silicon carbide has a carrier concentration of from about 1×10^{16} to about 1×10^{17} cm^{-3};

ohmic contacts on the n-type epitaxial layer that respectively define a source and a drain; and

a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain to form an active channel in the n-type epitaxial layer between the source and the drain when a bias is applied to the Schottky metal contact.

61. A transistor according to Claim 60, wherein the p-type epitaxial layer has a carrier concentration of from about 3×10^{16} to about 5×10^{16} cm^{-3}.

62. A transistor according to Claim 60, wherein the ohmic contacts are directly on the n-type epitaxial layer.

63. A transistor according to Claim 60, further comprising regions of n^+ silicon carbide between the n-type epitaxial layer and the ohmic contacts.

64. A transistor according to Claim 60, wherein the ohmic contacts comprise nickel contacts directly on the n-type epitaxial layer.

65. A transistor according to Claim 60 further comprising an overlayer on the ohmic contacts and the Schottky metal contact.

66. A transistor according to Claim 64, wherein the ohmic contacts comprise nickel and wherein the overlayer comprises layers of titanium, platinum and gold.

67. A transistor according to Claim 60, wherein the n-type epitaxial and p-type epitaxial layers form a mesa having sidewalls extending from the n-type layer into the p-type layer which define the periphery of the transistor.

68. A transistor according to Claim 67 wherein the mesa further comprises the substrate and the sidewalls of the mesa extend into the substrate.

69. A transistor according to Claim 67, further comprising a passivation layer on the sidewalls of the mesa and exposed portions of the n-type epitaxial layer.

70. A transistor according to Claim 69, wherein the passivation layer is an ONO passivation layer.

71. A transistor according to Claim 60, further comprising metallization formed on the substrate opposite the n-type layer.

72. A transistor according to Claim 71, wherein the substrate has a thickness of about 100 μm or less.

73. A transistor according to Claim 71, wherein the metallization comprises layers of titanium, platinum and gold coated with an overlayer of eutectic alloy of AuGe.

74. A transistor according to Claim 60 wherein the Schottky metal contact comprises a first gate layer of chromium directly on the n-type epitaxial layer.

75. A transistor according to Claim 74, wherein the Schottky metal contact further comprises an overlayer on the first gate layer, wherein the overlayer comprises layers of platinum and gold.

76. A transistor according to Claim 75, wherein the Schottky metal contact is a mushroom gate.

77. A transistor according to Claim 76, further comprising a recess in the n-type epitaxial layer and wherein the first gate layer is formed in the recess in the n-type epitaxial layer.

78. A transistor according to Claim 76, wherein the mushroom gate is self aligned with respect to the recess.

79. A transistor according to Claim 60, further comprising:

a cap layer of n-type silicon carbide on the n-type epitaxial layer;

a recess in the cap layer;

a recess in the n-type epitaxial layer, wherein the recess in the n-type epitaxial layer is within the recess in the cap layer; and

wherein the Schottky metal contact is within the recess in the n-type epitaxial layer.

80. A transistor according to Claim 79, wherein the recess in the n-type epitaxial layer extends to a depth of from about 20 nm to about 120 nm.

81. A transistor according to Claim 79, wherein the cap layer is doped at the same level as the n-type epitaxial layer.

82. A transistor according to Claim 79, wherein the cap layer has a dopant level from about 1×10^{15} cm^{-3} to about 5×10^{17} cm^{-3}.

83. A transistor according to Claim 79, wherein the cap layer has a thickness of from about 50 nm to about 300 nm.

84. A transistor according to Claim 60 wherein the substrate comprises semi-insulating silicon carbide.

85. A transistor according to Claim 84, wherein the semi-insulating silicon carbide is substantially free of deep level dopants.

86. A transistor according to Claim 60, further comprising a contact to the p-type epitaxial layer.

87. A transistor according to Claim 86, further comprising:

a p^+ well region formed in the p-type epitaxial layer; and

wherein the contact to the p-type epitaxial layer is formed on the p^+ well region.

88. A transistor according to Claim 86, wherein the p-type epitaxial layer comprises:

a first p-type conductivity silicon carbide layer formed on the substrate; and

a second p-type conductivity silicon carbide layer formed on the substrate, wherein the first p-type conductivity silicon carbide layer is more heavily doped than the second p-type conductivity silicon carbide layer.

89. A metal-semiconductor field-effect transistor comprising:

an n-type layer of n-type conductivity silicon carbide on a silicon carbide substrate;

ohmic contacts on the n-type layer and spaced apart that respectively define a source and a drain; and

a region of chromium on the n-type layer that is between the ohmic contacts and thereby between the source and the drain so as to provide a Schottky metal contact to form an active channel in the n-type layer between the source and the drain when a bias is applied to the Schottky metal contact.

90. A transistor according to Claim 89, further comprising a p-type layer of p-type conductivity silicon carbide between the substrate and the n-type layer.

91. A transistor according to Claim 90, further comprising an ohmic contact formed on the p-type epitaxial layer.

92. A transistor according to Claim 91, further comprising a well region of p^+ silicon carbide formed in the p-type layer and wherein the ohmic contact is formed on the p^+ well region.

93. A transistor according to Claim 91, wherein the p-type layer comprises:

a first p-type epitaxial layer; and

a second p-type epitaxial layer, wherein the first p-type epitaxial layer has a doping concentration higher than a doping concentration of the second p-type epitaxial layer.

94. A transistor according to Claim 89, regions of n^+ silicon carbide between the n-type epitaxial layer and the ohmic contacts.

95. A transistor according to Claim 89 further comprising an overlayer on the ohmic contacts and the Schottky metal contact.

96. A transistor according to Claim 95, wherein the ohmic contacts comprise nickel and wherein the overlayer comprises layers of titanium, platinum and gold.

97. A transistor according to Claim 90, wherein the n-type and p-type layers forms a mesa having sidewalls extending from the n-type layer into the p-type layer which define the periphery of the transistor.

98. A transistor according to Claim 97 wherein the mesa further comprises the substrate and the sidewalls of the mesa extend into the substrate.

99. A transistor according to Claim 97, further comprising a passivation layer on the sidewalls of the mesa and exposed portions of the n-type epitaxial layer.

100. A transistor according to Claim 99, wherein the passivation layer is an ONO passivation layer.

101. A transistor according to Claim 89, further comprising metallization on the substrate opposite the n-type layer.

102. A transistor according to Claim 101, wherein the substrate has a thickness of 100 μm or less.

103. A transistor according to Claim 101, wherein the metallization comprises layers of titanium, platinum and gold coated with an overlayer of eutectic alloy of AuGe.

104. A transistor according to Claim 97, wherein the Schottky metal contact further comprises an overlayer on the chromium region, wherein the overlay comprises layers of platinum and gold.

105. A transistor according to Claim 89, wherein the Schottky metal contact is a mushroom gate.

106. A transistor according to Claim 89, further comprising a recess in the n-type layer and wherein the chromium region is in the recess in the n-type layer.

107. A transistor according to Claim 106, wherein the chromium region is self aligned.

108. A transistor according to Claim 89, wherein the ohmic contacts are directly on the n-type epitaxial layer.

109. A metal-semiconductor field-effect transistor comprising:

a bulk single crystal silicon carbide substrate;

an n-type epitaxial layer of n-type conductivity silicon carbide on the substrate;

ohmic contacts on the n-type epitaxial layer that respectively define a source and a drain;

a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain to form an active

channel in the n-type epitaxial layer between the source and the drain when a bias is applied to the Schottky metal contact;

wherein the n-type epitaxial layer forms a mesa having sidewalls extending into the n-type layer which define the periphery of the transistor; and

an ONO passivation layer on the sidewalls of the mesa and exposed portions of the n-type epitaxial layer.

110. A transistor according to Claim 109 wherein the mesa further comprises the substrate and the sidewalls of the mesa extend into the substrate.

111. A transistor according to Claim 109, further comprising:

a p-type epitaxial layer of p-type conductivity silicon carbide between the substrate and the n-type epitaxial layer; and

wherein the sidewalls of the mesa extends from the n-type layer into the p-type layer.

112. A transistor according to Claim 111, further comprising an ohmic contact formed on the p-type epitaxial layer.

113. A transistor according to Claim 112, further comprising a well region of p^+ silicon carbide formed in the p-type epitaxial layer and wherein the ohmic contact is formed on the p^+ well region.

114. A transistor according to Claim 112, wherein the p-type epitaxial layer comprises:

a first p-type epitaxial layer; and

a second p-type epitaxial layer, wherein the first p-type epitaxial layer has a doping concentration higher than a doping concentration of the second p-type epitaxial layer.

115. A transistor according to Claim 109, wherein the ohmic contacts are directly on the n-type epitaxial layer.

116. A transistor according to Claim 109, further comprising regions of n^+ silicon carbide between the n-type epitaxial layer and the ohmic contacts.

117. A transistor according to Claim 109, wherein the ohmic contacts comprise nickel contacts directly on the n-type epitaxial layer.

118. A transistor according to Claim 109 further comprising an overlayer on the ohmic contacts and the Schottky metal contact.

119. A transistor according to Claim 118, wherein the ohmic contacts comprise nickel and wherein the overlayer comprises layers of titanium, platinum and gold.

120. A transistor according to Claim 109, further comprising metallization formed on the substrate opposite the n-type layer.

121. A transistor according to Claim 120, wherein the substrate has a thickness of about 100 μm or less.

122. A transistor according to Claim 120, wherein the metallization comprises layers of titanium, platinum and gold coated with an overlayer of eutectic alloy of AuGe.

123. A transistor according to Claim 109, wherein the Schottky metal contact is a mushroom gate.

124. A transistor according to Claim 109, further comprising a recess in the n-type epitaxial layer and wherein the gate contact is formed in the recess in the n-type epitaxial layer.

125. A transistor according to Claim 124, wherein the gate contact is a self aligned gate contact.

126. A metal-semiconductor field-effect transistor comprising:

a semi-insulating silicon carbide substrate which is substantially free of deep level dopants;

a buffer layer of silicon carbide on the semi-insulating silicon carbide substrate;

an n-type epitaxial layer on the buffer layer;

a cap layer on the n-type epitaxial layer;

ohmic contacts on the n-type epitaxial layer that respectively define a source and a drain;

a first recess in the cap layer between the source and drain contacts;

a second recess in the n-type epitaxial layer within the first recess;

a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain to form an active channel in the n-type epitaxial layer between the source and the drain when a bias is applied to the Schottky metal contact, wherein the Schottky metal contact includes a layer of chromium on the n-type epitaxial layer in the second recess;

wherein the n-type epitaxial layer forms a mesa having sidewalls extending into the n-type layer which define the periphery of the transistor; and

an ONO passivation layer on the sidewalls of the mesa and exposed portions of the n-type epitaxial layer.

127. A transistor according to Claim 126, wherein the buffer layer comprises a p-type epitaxial layer of selectively doped p-type conductivity silicon carbide between the substrate and the n-type epitaxial layer, wherein the p-type conductivity silicon carbide has a carrier concentration of from about 1×10^{16} to about 1×10^{17} cm^{-3}.

128. A transistor according to Claim 126, wherein the buffer layer comprises undoped silicon carbide.

129. A method of fabricating a passivation layer of a silicon carbide semiconductor device, comprising:

forming an oxide layer on the silicon carbide semiconductor device; and then annealing the oxide layer in a NO environment.

130. A method according to Claim 129, wherein the step of forming an oxide layer comprises the step of thermally growing an oxide layer.

131. A method according to Claim 129, wherein the step of forming an oxide layer comprises the step of depositing an oxide layer on the silicon carbide semiconductor device.

132. A method according to Claim 129, wherein the passivation layer is an ONO passivation layer, and wherein the annealing step is followed by the steps of:

depositing a layer of Si_3N_4 on the oxidized SiO_2 layer; then

oxidizing the layer of Si_3N_4.

133. A method according to Claim 132, wherein the step of forming an oxide layer comprises the steps of:

high temperature annealing exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer in an H_2 ambient; then

forming an SiO_2 layer on the exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer; then

argon annealing the SiO_2 layer; then

oxidizing the SiO_2 layer.

134. A method of fabricating a metal-semiconductor field-effect transistor comprising:

forming a p-type epitaxial layer of selectively doped p-type conductivity silicon carbide on a single crystal silicon carbide substrate, wherein the p-type conductivity silicon carbide has a carrier concentration of from about 1×10^{16} to about 1×10^{17} cm^{-3}; then

forming an n-type epitaxial layer of n-type conductivity silicon carbide on the p-type epitaxial layer, wherein the n-type epitaxial forms a mesa having sidewalls extending into the n-type layer which define the periphery of the transistor;

forming ohmic contacts on the n-type epitaxial layer that respectively define a source and a drain; and

forming a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain; and

forming an ONO passivation layer on the sidewalls of the mesa and exposed portions of the n-type epitaxial layer.

135. A method according to Claim 134 further comprising the step of etching the n-type epitaxial layer and the p-type epitaxial layer to form a mesa.

136. A method according to Claim 134, wherein the steps of forming ohmic contacts and forming a Schottky gate contact are preceded by the steps of:

etching the n-type epitaxial layer and the p-type epitaxial layer to form a mesa; and

forming an ONO passivation layer on the exposed surfaces of the mesa.

137. A method according to Claim 136, wherein the step of forming an ONO passivation layer comprises the steps of:

high temperature annealing exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer in an H_2 ambient; then

forming an SiO_2 layer on the exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer; then

argon annealing the SiO_2 layer; then

oxidizing the SiO_2 layer; then

depositing a layer of Si_3N_4 on the oxidized SiO_2 layer; then

oxidizing the layer of Si_3N_4.

138. A method according to Claim 137, wherein the high temperature anneal is carried out at a temperature of greater than about 900 °C for a time of from about 15 minutes to about 2 hours.

139. A method according to Claim 137, wherein the argon anneal is carried out at a temperature of about 1200 °C for a time of about 1 hour.

140. A method according to Claim 137, wherein the step of forming an SiO_2 layer comprises the step of forming an SiO_2 layer to a thickness of from about 50 to about 500 Å.

141. A method according to Claim 137, wherein the step of forming an SiO_2 layer comprises forming an SiO_2 layer through a dry oxide process at a temperature of about 1200 °C.

142. A method according to Claim 137, wherein the step of oxidizing the SiO_2 layer comprises the step of oxidizing the SiO_2 layer in a wet environment at a temperature of about 950 °C for a time of about 180 minutes.

143. A method according to Claim 137, wherein the step of depositing a layer of Si_3N_4 comprises the step of depositing a layer of Si_3N_4 to a thickness of from about 200 to about 2000 Å.

143. A method according to Claim 137, wherein the step of depositing a layer of Si_3N_4 comprises the step of depositing a layer of Si_3N_4 through chemical vapor deposition.

144. A method according to Claim 137, wherein the step of oxidizing the layer of Si_3N_4 comprises the step of oxidizing the Si_3N_4 layer in a wet environment at a temperature of about 950 °C for a time of about 180 minutes.

145. A method according to Claim 137, wherein the step of oxidizing the layer of Si_3N_4 comprises the step of oxidizing the Si_3N_4 layer to provide an oxide layer having a thickness of from about 20 to about 200 Å.

146. A method according to Claim 137, wherein the step of depositing a layer of Si_3N_4 on the oxidized SiO_2 layer is preceded by the step of annealing the oxidized SiO_2 layer in a NO environment.

147. A method according to Claim 134, further comprising the step of forming a gate recess in the n-type epitaxial layer and wherein the step of forming a

Schottky gate contact comprises the step of forming a Schottky gate contact in the gate recess.

148. A method according to Claim 147, further comprising the step of:

etching through the ONO passivation layer and into the n-type epitaxial layer so as to provide a gate recess in the n-type epitaxial layer; and

wherein the step of forming a Schottky gate contact comprises the step of forming a Schottky gate contact in the gate recess utilizing the ONO passivation layer as a mask.

149. A method according to Claim 148, wherein the step of etching through the ONO passivation layer is followed by the step of patterning the ONO passivation layer so as to provide a ledge in sidewalls of the opening of the ONO passivation layer for the gate recess; and

wherein the step of forming a Schottky gate contact in the gate recess comprises the step of forming a mushroom gate structure in the gate recess and on the sidewalls and ledge of the ONO passivation layer.

150. A method according to Claim 148, wherein the step of etching through the ONO passivation layer is carried out by at least one of Electron Cyclotron Resonance and Inductively Coupled Plasma etching.

151. A method according to Claim 147, wherein the step of forming a gate recess is preceded by the steps of:

forming a cap layer of silicon carbide on the n-type epitaxial layer;

etching through the cap layer to provide a first recess;

wherein the step of forming an ONO passivation layer comprises forming an ONO passivation layer on the cap layer;

etching through the ONO passivation layer and into the n-type epitaxial layer so as to provide a second recess in the n-type epitaxial layer, wherein the second recess is within the first recess; and

wherein the step of forming a Schottky gate contact comprises the step of forming a Schottky gate contact in the second recess utilizing the ONO passivation layer as a mask.

152. A method according to Claim 134, further comprising the step of implanting n^+ well regions in the n-type epitaxial layer so as to provide source and drain regions and wherein the step of forming ohmic contacts comprises the step of forming ohmic contacts on the n^+ well regions.

153. A method according to Claim 134, further comprising the steps of:

thinning the substrate; and then

forming a metallization layer on the substrate opposite the p-type epitaxial layer.

154. A method according to Claim 153, wherein the step of forming a metallization layer comprises the steps of:

forming a titanium layer on the substrate opposite the p-type epitaxial layer; then

forming a layer of platinum on the titanium layer; and then

forming a layer of gold on the layer of platinum.

155. A method according to Claim 153, further comprising the step of forming a layer of a eutectic alloy of AuGe on the layer of gold.

156. A method of fabricating a gate structure for a silicon carbide field effect transistor comprising the steps of:

forming an ONO passivation layer on exposed surfaces of a mesa terminated silicon carbide field effect transistor;

forming a gate window in the ONO passivation layer;

forming a gate recess in a channel layer of the mesa terminated silicon carbide transistor;

forming a gate contact in the gate recess in the channel layer.

157. A method according to Claim 156, wherein the step of forming an ONO passivation layer comprises the steps of:

high temperature annealing exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer in an H_2 ambient; then

forming an SiO_2 layer on the exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer; then

argon annealing the SiO_2 layer; then

oxidizing the SiO_2 layer; then

depositing a layer of Si_3N_4 on the oxidized SiO_2 layer; then

oxidizing the layer of Si_3N_4.

158. A method according to Claim 157, wherein the step of depositing a layer of Si_3N_4 on the oxidized SiO_2 layer is preceded by the step of annealing the oxidized SiO_2 layer in a NO environment.

159. A method according to Claim 157, wherein the high temperature anneal is carried out at a temperature of greater than about 900 °C for a time of from about 15 minutes to about 2 hours.

160. A method according to Claim 157, wherein the argon anneal is carried out at a temperature of about 1200 °C for a time of about 1 hour.

161. A method according to Claim 157, wherein the step of forming an SiO_2 layer comprises the step of forming an SiO_2 layer to a thickness of from about 50 to about 500 Å.

162. A method according to Claim 157, wherein the step of forming an SiO_2 layer comprises forming an SiO_2 layer through a dry oxide process at a temperature of about 1200 °C.

163. A method according to Claim 157, wherein the step of oxidizing the SiO_2 layer comprises the step of oxidizing the SiO_2 layer in a wet environment at a temperature of about 950 °C for a time of about 180 minutes.

164. A method according to Claim 157, wherein the step of depositing a layer of Si_3N_4 comprises the step of depositing a layer of Si_3N_4 to a thickness of from about 200 to about 2000 Å.

165. A method according to Claim 157, wherein the step of depositing a layer of Si_3N_4 comprises the step of depositing a layer of Si_3N_4 through chemical vapor deposition.

166. A method according to Claim 157, wherein the step of oxidizing the layer of Si_3N_4 comprises the step of oxidizing the Si_3N_4 layer in a wet environment at a temperature of about 950 °C for a time of about 180 minutes.

167. A method according to Claim 157, wherein the step of oxidizing the layer of Si_3N_4 comprises the step of oxidizing the Si_3N_4 layer to provide an oxide layer having a thickness of from about 20 to about 200 Å.

168. A method according to Claim 156, wherein the step of forming a gate contact comprises the step of forming a gate contact in the gate recess utilizing the ONO passivation layer as a mask.

169. A method according to Claim 168, further comprising the step of patterning the ONO passivation layer so as to provide a ledge in sidewalls of the opening of the ONO passivation layer for the gate recess; and

wherein the step of forming a gate contact in the gate recess comprises the step of forming a mushroom gate structure in the gate recess and on the sidewalls and ledge of the ONO passivation layer.

170. A method according to Claim 156, wherein the steps of forming a gate window and forming a gate recess are carried out by etching through the ONO passivation layer and into the channel layer by at least one of Electron Cyclotron Resonance and Inductively Coupled Plasma etching.

171. A method of forming a metal-semiconductor field-effect transistor, comprising:

forming an n-type epitaxial layer of n-type conductivity silicon carbide on a silicon carbide substrate;

forming ohmic contacts on the n-type epitaxial layer that respectively define a source and a drain;

forming a cap layer of n-type silicon carbide on the n-type epitaxial layer;

forming a first recess in the cap layer;

forming a second recess in the n-type epitaxial layer, wherein the recess in the n-type epitaxial layer is within the first recess in the cap layer; and

forming a Schottky metal contact on the n-type epitaxial layer that is between the ohmic contacts and thereby between the source and the drain to form an active channel in the n-type epitaxial layer between the source and the drain when a bias is applied to the Schottky metal contact wherein the Schottky metal contact is within the recess in the n-type epitaxial layer.

172. A method according to Claim 171, wherein the steps of forming an n-type epitaxial layer and forming a cap layer comprises the step of epitaxially growing the n-type epitaxial layer and the cap layer in a single growth step.

173. A method according to Claim 172, wherein an n-type dopant concentration in the single growth step is changed to grow the cap layer.

174. A method according to Claim 171, wherein the step of forming a first recess in the cap layer comprises the step of patterning the cap layer to form the first recess.

175. A method according to Claim 172, further comprising the steps of:

forming a mesa having sidewalls which extend through the cap layer and the n-type epitaxial layer; and

wherein the step of patterning the cap layer to form the first recess is followed by the steps of:

forming an ONO passivation layer on exposed surfaces of the mesa and the first recess;

forming a gate window in the ONO passivation layer, wherein the gate window is within the first recess;

forming the second recess in n-type epitaxial layer; and

forming a gate contact in the second recess.

176. A method according to Claim 175, wherein the step of forming an ONO passivation layer comprises the steps of:

high temperature annealing exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer in an H_2 ambient; then

forming an SiO_2 layer on the exposed portions of the substrate, p-type epitaxial layer and n-type epitaxial layer; then

argon annealing the SiO_2 layer; then

oxidizing the SiO_2 layer; then

depositing a layer of Si_3N_4 on the oxidized SiO_2 layer; and then

oxidizing the layer of Si_3N_4.

177. A method according to Claim 176, wherein the step of depositing a layer of Si_3N_4 on the oxidized SiO_2 layer is preceded by the step of annealing the oxidized SiO_2 layer in a NO environment.

178. A method according to Claim 175, wherein the step of forming a gate contact comprises the step of forming a gate contact in the second recess utilizing the ONO passivation layer as a mask.

179. A method according to Claim 178, wherein the step of forming a gate contact in the second recess comprises the step of forming a mushroom gate structure in the second recess.

180. A method according to Claim 175, wherein the steps of forming a gate window and forming a second recess are carried out by etching through the ONO passivation layer and into the n-type epitaxial layer by at least one of Electron Cyclotron Resonance and Inductively Coupled Plasma etching.

181. A method according to Claim 171, wherein the step of forming a substrate comprises the step of forming a semi-insulating SiC substrate which is substantially free of deep-level dopants.

182. A method according to Claim 171, further comprising the step of forming a buffer layer between the substrate and the n-type epitaxial layer.

183. A method according to Claim 182, wherein the step of forming a buffer layer comprises the step of forming an undoped silicon carbide epitaxial layer.

184. A method according to Claim 182, wherein the step of forming a buffer layer comprises the step of forming an n-type silicon carbide epitaxial layer.

185. A method according to Claim 182, wherein the step of forming a buffer layer comprises the step of forming a p-type silicon carbide epitaxial layer.

186. A method according to Claim 183, wherein the step of forming a p-type epitaxial layer comprises the steps of:

forming a first p-type epitaxial layer on the substrate; and

forming a second p-type epitaxial layer on the first p-type epitaxial layer, wherein the second p-type epitaxial layer has a lower dopant concentration than the first p-type epitaxial layer.

187. A method according to Claim 185, further comprising the step of forming an ohmic contact to the p-type epitaxial layer.

188. A method according to Claim 187, further comprising the step of implanting p-type dopants in the p-type epitaxial layer so as to provide a region of p-type conductivity silicon carbide having a higher carrier concentration than the p-type epitaxial layer; and

wherein the step of forming an ohmic contact comprises the step of forming an ohmic contact on the implanted region.

189. A method according to Claim 187, wherein the step of forming an ohmic contact comprises the steps of:

etching a ground contact window through the cap layer and the n-type epitaxial layer in a region adjacent a source region of the MESFET; and

forming the ohmic contact in the ground contact window.